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Microprocessor
Third Stage

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8085 Machine Cycles and their Timings:

The 8085 has five machine cycle. These are:
1. Opcode fetch.
2. Memory read.
3. Memory write.
4. I/O read.
5. I/O write.

1. **Opcode Fetch Cycle:**

The first machine cycle of every instruction is opcode fetch cycle in which the 8085 finds the nature of the instruction to be executed. In this machine cycle, the microprocessor places the contents of PC on the address bus then by reading operation it reads the opcod of an instruction from determined memory location. The length of this cycle is not fixed. Steps below explain opcode fetch cycle in

more details. Figure 1 shows the timing diagram and data flow of opcod fetch cycle.

> **Step1: (T_1 state)** The 8085 processor places the contents of program counter on the address bus, activate the ALE and send the status signals $IO/\overline{M}$, S_1, and S_0 with logical status (0 1 1) respectively.

> **Step 2: (T_2 state)** The low order address disappears from AD_0-AD_7 lines. Also, 8085 processor activates the $\overline{RD}$ signals to enable the addressed memory location which places its contents on the data bus (AD_0-AD_7).

> **Step 3: (T_3 state)** The processor loads the contents of data bus on its Instruction Register and deactivates the $\overline{RD}$ signal to disables the memory devices.

> **Step4: (T_4 state)** the processor decode the opcode, and on the basis of the instruction received, it decides whether to enter T_5 or to enter T_1 of new machine cycle. One byte instructions those operate on eight bit data (8 bit operand) are executed in T_4. for example: MOV C,B- ANA E- ADD B- INR C- RAR …etc.

> **Step5: (T_5 & T_6 states)** the processor performs stack write, internal 16 bits, or conditional return operations depending upon the type of instruction. One byte instructions those operate on 16 bit data are executed in T_5 & T_6. For example DCX H, PCHL, SPHL, INX H, etc.

(a) Data (opcode) flow from memory to micrprocessor

(b) Opcode fetch machine cycle

Figure 1 details of opcode machine cycle.

2 Memory read cycle:

The microprocessor executes the memory read cycle to read the data from RAM or ROM memory. 8085 processor executes this machine cycle in 3 T-states. Steps below show the details of this machine cycle:

➢ **Step1 (T_1 state):** processor places the address on the address lines from SP, Rp, or PC and activates ALE in order to latch low-order of address. Also, it sends the status signals with logical status (0 1 0) for memory read machine cycle.

➢ **Step2 (T_2 state):** , 8085 processor activates the $\overline{RD}$ signals to enable the addressed memory location which places its contents on the data bus (AD_0-AD_7).

➢ **Step 3: (T_3 state)** The processor loads the contents of data bus on specified register (F, A, B, C, D, E, H, and L) and deactivates the $\overline{RD}$ signal to disables the memory devices.

Figure 2 shows the timing diagram and data follow for read memory machine cycle.

(a) Data flow from memory to microprocessor   (b) Memory read machine cycle
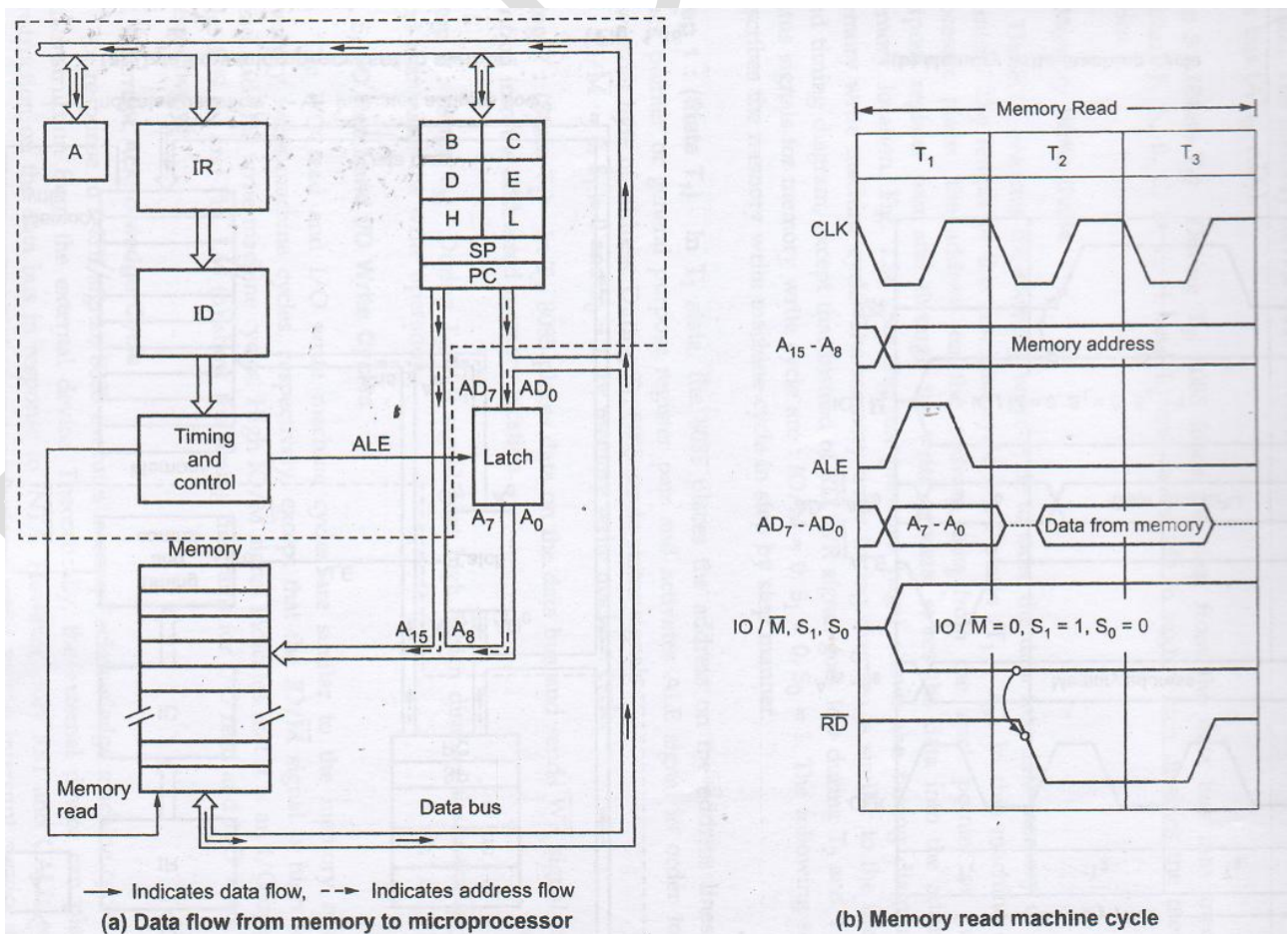
Figure 2: details of memory read machine cycle.

3 - Memory write cycle:

The microprocessor executes the memory write cycle to store the data into RAM or stack memory. 8085 processor executes this machine cycle in 3 T-states. Steps below show the details of this machine cycle:

➢ **Step1 (T_1 state):** processor places the address on the address lines from SP or Rp and activates ALE in order to latch low-order of address. Also, it sends the status signals with logical status (0 0 1) for memory write machine cycle.

➢ **Step2 (T_2 state):** , 8085 processor places tha data on data bus and activates the $\overline{WR}$ signal to writing data into addressed memory location.

➢ **Step 3: (T_3 state)** The processor deactivates the $\overline{WR}$ signal which disables the memory device and terminates the write operation.

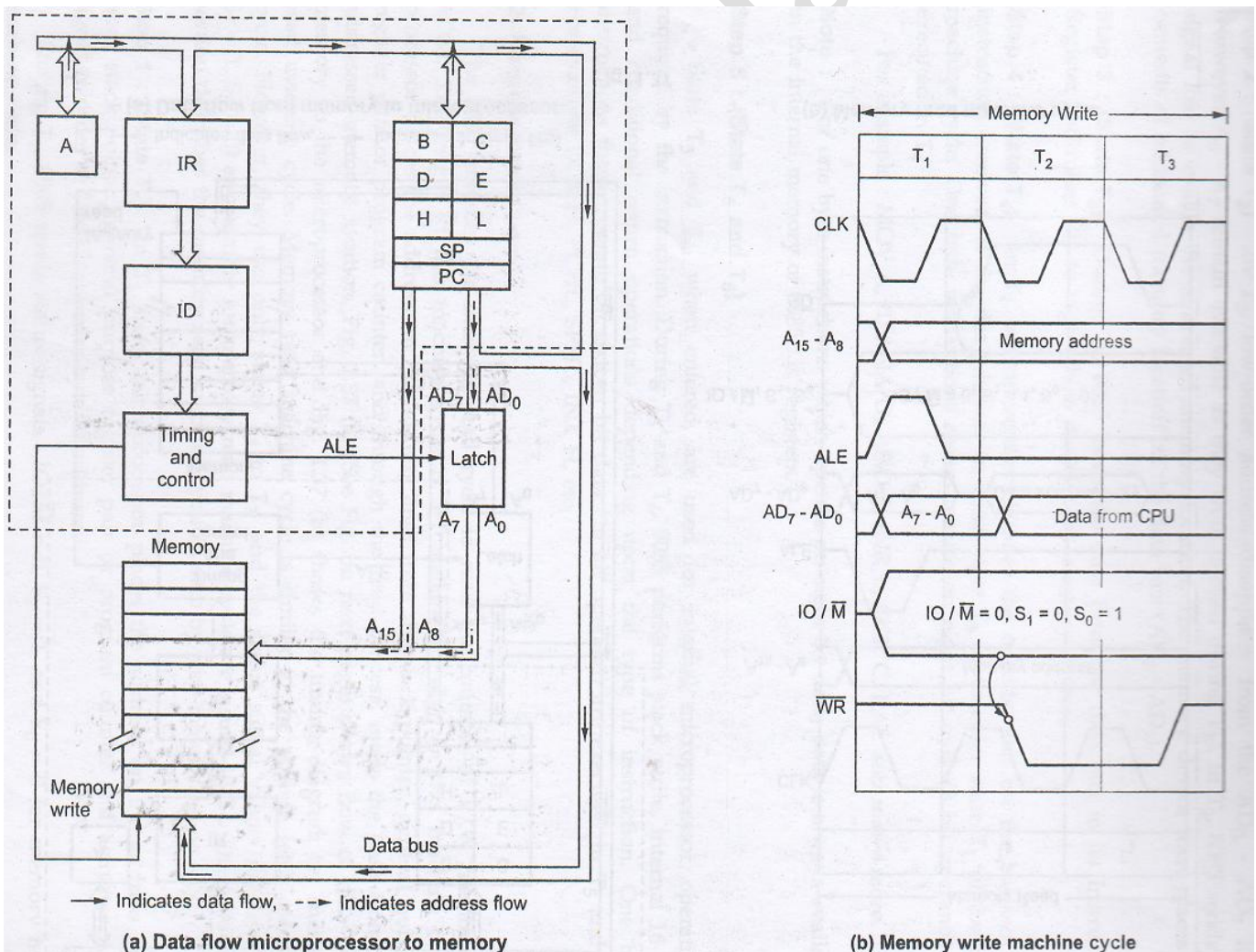Figure 3 shows the timing diagram and data follow for memory write machine cycle.

(a) Data flow microprocessor to memory

(b) Memory write machine cycle

Figure 3: details of memory write machine cycle.

4 IO read cycle:

The microprocessor executes the IO read cycle to read the data from input device. 8085 processor executes this machine cycle in 3 T-states. Steps below show the details of this machine cycle:

➢ **Step1 (T_1 state):** processor places the address on the address lines from SP, Rp, or PC and activates ALE in order to latch low-order of address. Also, it sends the status signals with logical status (1 1 0) for IO read machine cycle.

➢ **Step2 (T_2 state):** , 8085 processor activates the $\overline{RD}$ signals to enable the addressed input device which places its contents on the data bus (AD_0-AD_7).

➢ **Step 3: (T_3 state)** The processor loads the contents of data bus on specified register (F, A, B, C, D, E, H, and L) and deactivates the $\overline{RD}$ signal to disables the input device.

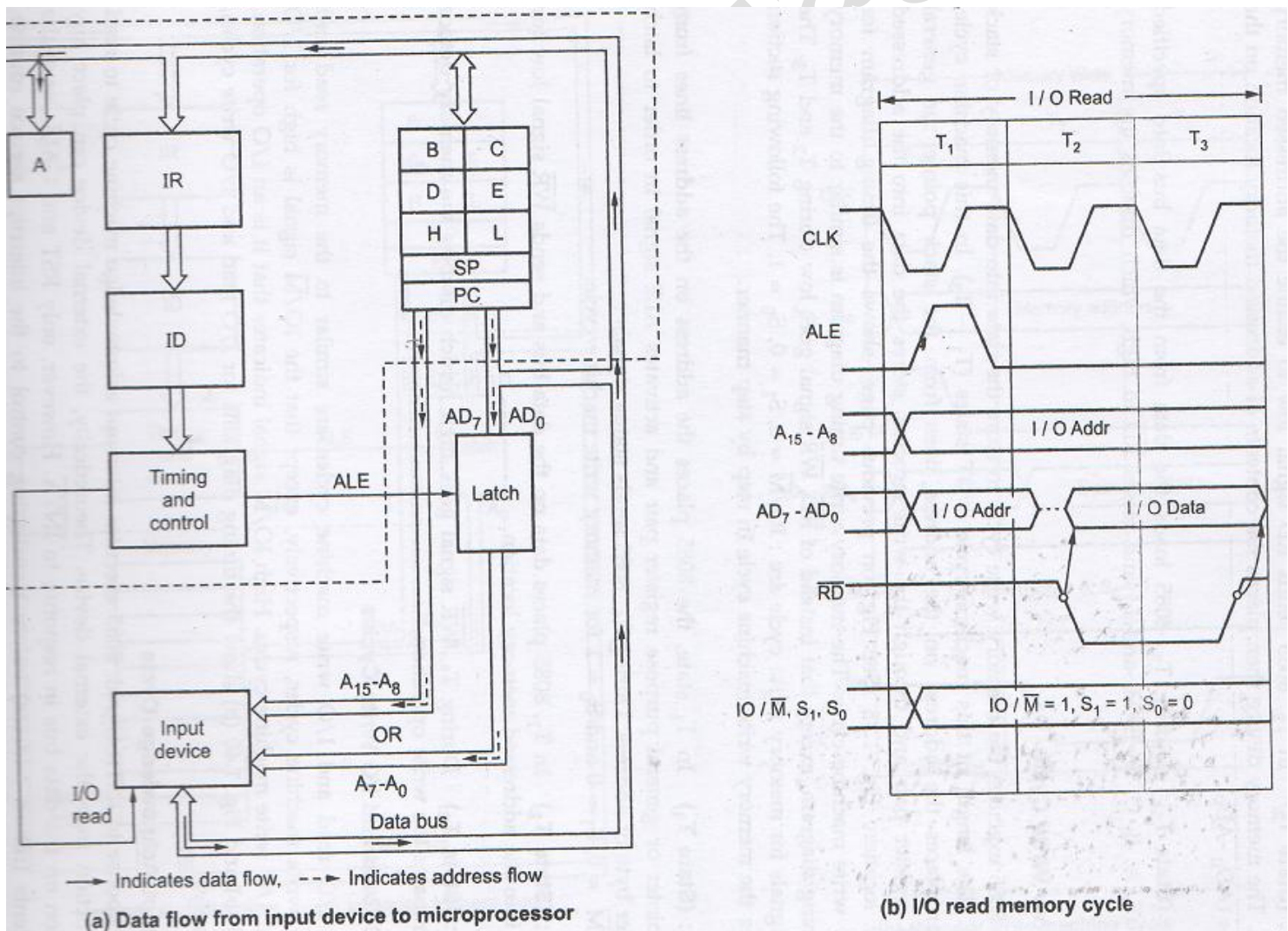Figure 4 shows the timing diagram and data follow for IO read machine cycle.

(a) Data flow from input device to microprocessor

(b) I/O read memory cycle

— Indicates data flow, --► Indicates address flow

Figure4   IO read machine cycle.

5 - IO write cycle:

The microprocessor executes the IO write cycle to store the data into output device. 8085 processor executes this machine cycle in 3 T-states. Steps below show the details of this machine cycle:

➢ **Step1 (T_1 state):** processor places the address on the address lines from SP or Rp and activates ALE in order to latch low-order of address. Also, it sends the status signals with logical status (1 0 1) for IO write machine cycle.

➢ **Step2 (T_2 state):** , 8085 processor places the data on data bus and activates the $\overline{WR}$ signal to writing data into addressed output device.

➢ **Step 3: (T_3 state)** The processor deactivates the $\overline{WR}$ signal which disables the output device and terminates the writing operation.

Figure 5 shows the timing diagram and data follow for IO write machine cycle.
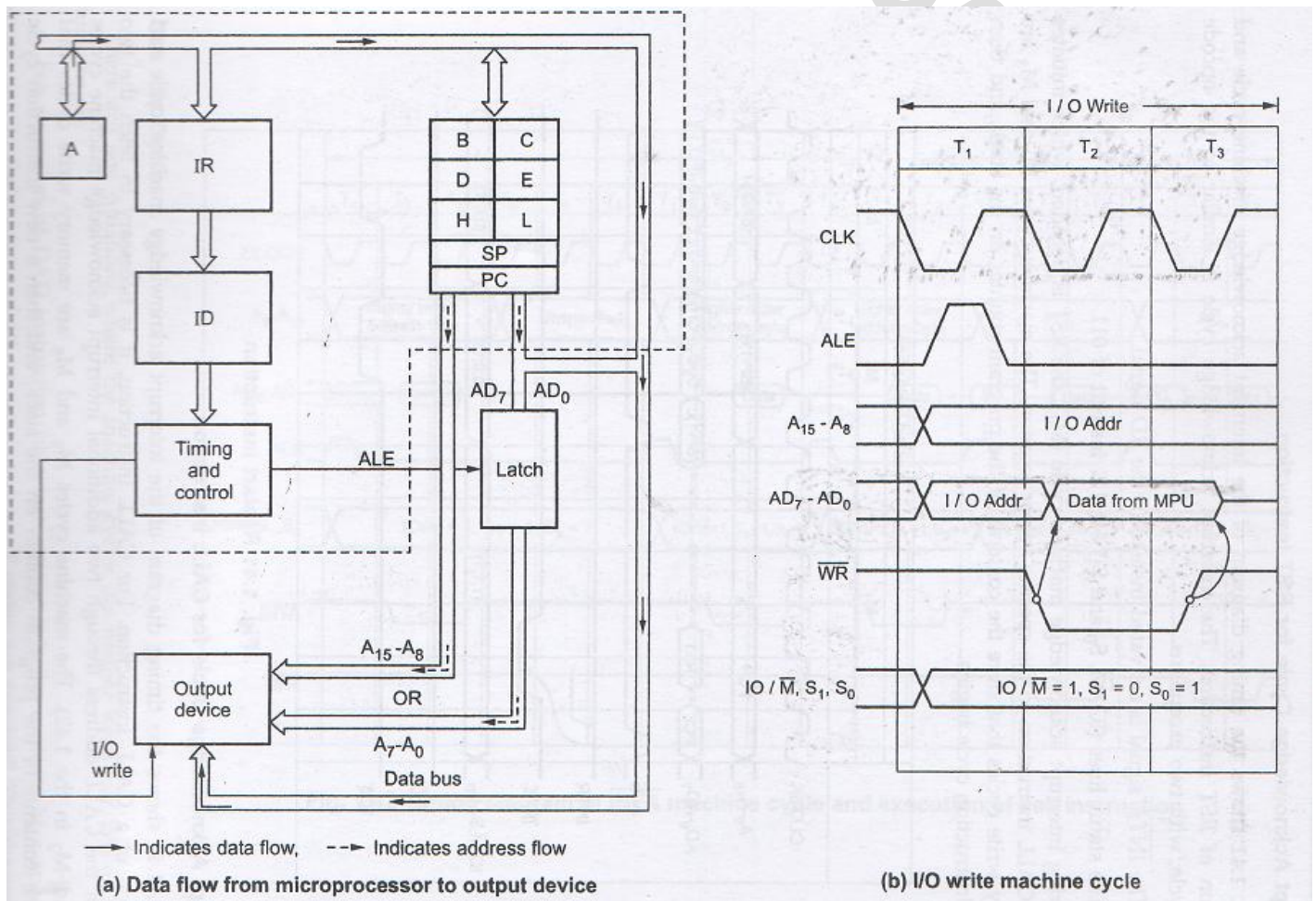

(a) Data flow from microprocessor to output device

(b) I/O write machine cycle

Figure 5: IO write machine cycle.